AMENDMENTS TO THE DRAWINGS

The attached sheet(s) of drawings includes changes to the formula for $Al_yIn_xGa_{1-(x+y)}N/In_xGa_{1-x}N/GaN$ so as to correspond to the amendments to the specification.

Attachment: Replacement sheets
Annotated sheets showing changes

REMARKS

The Examiner is thanked for the thorough examination of the application. A substitute Abstract has been provided.

The specification, claims and drawings have been amended to correct an obvious typographical error that would be clear to one of ordinary skill in the art. That is, one of ordinary skill would realize that the term "$Ga_{1-x,y}$" has no chemical meaning and that the term "$Ga_{1-(x+y)}$" was meant. As a result, no new matter is present in the application.

Status Of The Claims

Claims 1-20 are pending in the application. Claims 1, 4, 6 and 12 are independent. The claims have been amended to improve their language, to correct minor errors and to better set forth the invention being claimed.

Rejections Based On Emerson

Claims 1-13 and 16-20 have been rejected under 35 U.S.C. §102(e) as being anticipated by Emerson (U.S. Patent 6,958,497). Claims 14 and 15 have been rejected under 35 U.S.C. §103(a) as being obvious over Emerson in view of Yuasa (U.S. Patent 6,017,774). Applicant traverses.

The present invention pertains to a nitride semiconductor LED that includes $Al_yGa_{1-y}N/GaN$ ($0 < y \leq 1$) short period superlattice (SPS) layers **204**, **206** formed over a GaN-based buffer layer (see claims 1, 4 and 12).

Emerson pertains to Group II based LED structures. In the Office Action, the Examiner points to Figure 2 of Emerson (reproduced below), which includes an SiC substrate **10**, a buffer layer **11**, superlattice layers **16**, barrier layers **118**, and an active region **125**.

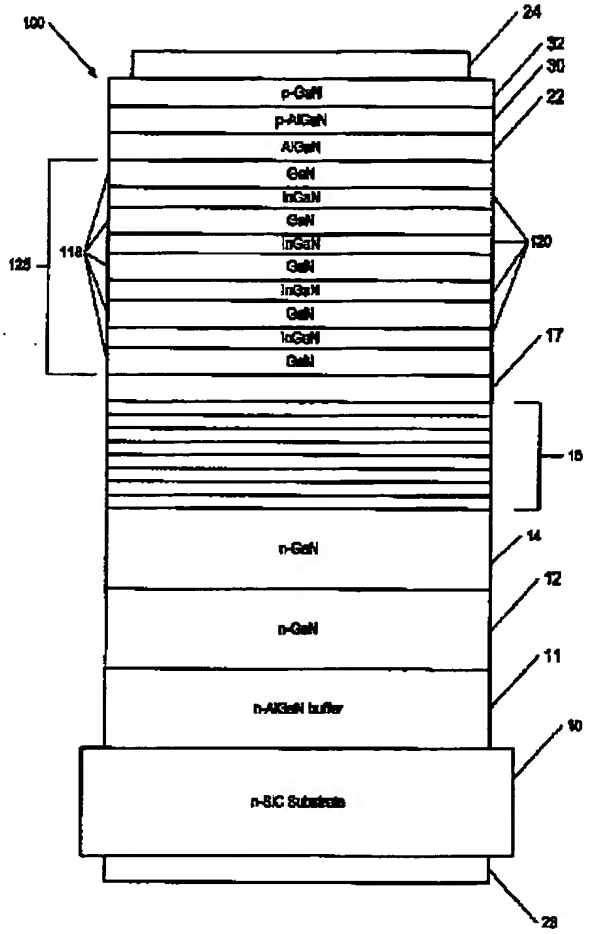

Fig. 2 of Emerson

Emerson fails to disclose or suggest $Al_yGa_{1-y}N$. Emerson's buffer layer **11** is not $Al_yGa_{1-y}N$ on a GaN-based buffer layer, but is rather an n-AlGaN buffer layer (column 8, line 52) used as a conductive buffer layer (column 6, lines 55-56). As a result, these features of Emerson are fundamentally different from the $Al_yGa_{1-y}N$ on a GaN-based buffer layer, as is set forth in the present invention.

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That is, the claimed invention includes a first electrode layer **207** of an n-GaN layer formed on the upper $Al_yGa_{1-y}N$/GaN short period superlattice (SPS) layer **206**. In contrast, Emerson's lowest GaN of the barrier layer **118** functions to separate the barrier layer **118** from the quantum well layer **120** (column 8, line 62 to column 9, line 14). As a result, Emerson fails to disclose the claimed first electrode layer **207** of the present invention.

Emerson thus fails to anticipate independent claims 1, 4, 6 and 12 of the present invention. Claims depending upon these independent claims are patentable for at least the above reasons.

At page 6 of the Office Action the Examiner turns to the teachings of Yuasa (pertaining to nitride film formation) to reject claims 14 and 15. However, these teachings of Yuasa fail to address the deficiencies of Emerson in teaching or suggesting a claimed embodiment of the present invention. A *prima facie* case of obviousness has thus not been made.

These rejections are overcome and withdrawal thereof is respectfully requested.

Information Disclosure Statement

The Examiner is thanked for considering the Information Disclosure Statement filed December 14, 2004 and for making the initialed PTO/SB/08 form of record in the application in the Office Action mailed May 9, 2006.

Prior Art

The prior art cited but not utilized by the Examiner indicates the status of the conventional art that the invention supersedes. Additional remarks are accordingly not necessary.

Foreign Priority

The Examiner has acknowledged foreign priority in the Office Action mailed May 9, 2006.

The Drawings

The Examiner is respectfully requested to indicate whether the replacement drawing figures are acceptable in the next official action.

Conclusion

The Examiner's rejections have been overcome, obviated or rendered moot. No issues remain. It is believed that a full and complete response has been made to the outstanding Office Action. The Examiner is accordingly respectfully requested to place the application in condition for allowance and to issue a Notice of Allowability.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert E. Goozner (Reg. No. 42,593) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

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If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.14; particularly, extension of time fees.

Dated: September 11, 2006

Respectfully submitted,

REG

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Attachments: Replacement Figs. 1-3

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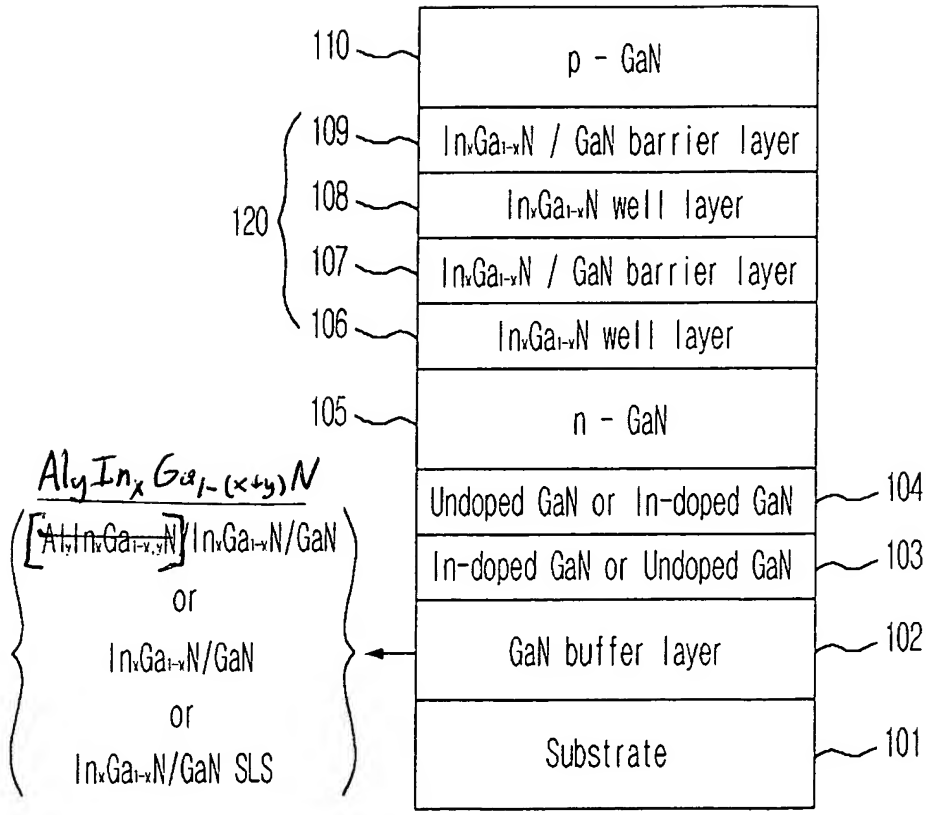
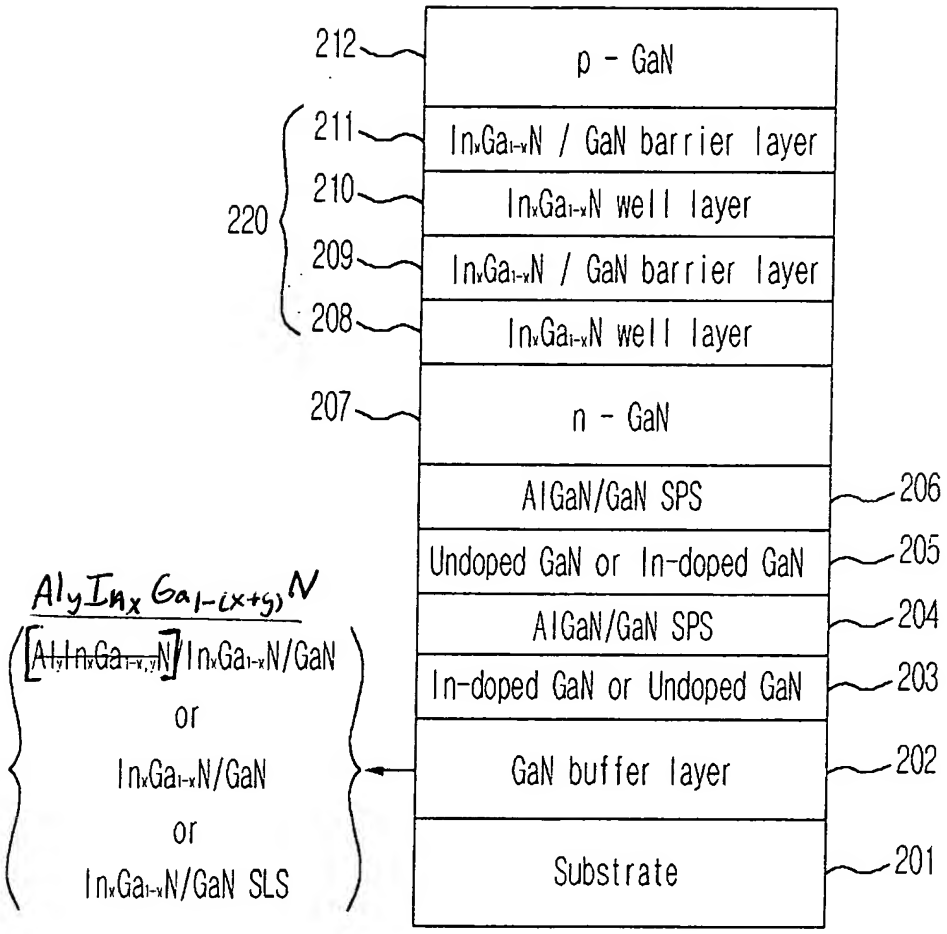
[FIG. 1



[FIG. 2]



[FIG. 3]